

TBA520

PAL TV CHROMA DEMODULATOR

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The TBA520 is a synchronous demodulator for direct drive of color video output stages. It is constructed on a single silicon chip using the Fairchild Planar* epitaxial process. The TBA520 is designed for use in color television receivers, operating on the Phase Alternate Line (PAL) system. This circuit consists of two synchronous demodulators, a decoding matrix and a PAL switch with internal multivibrator.

- DOUBLE BALANCED SYNCHRONOUS DEMODULATOR
- INTERNAL DECODING MATRIX
- INTERNAL PAL SWITCH
- PROVISION FOR OUTPUT DC LEVEL MATCHING

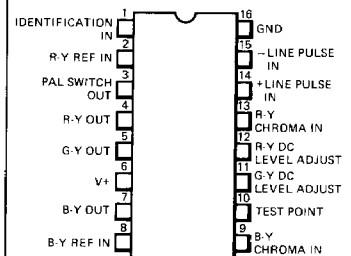
ABSOLUTE MAXIMUM RATINGS

Supply Voltage
Internal Power Dissipation
Voltage on Identification Input
Current into Identification Input
Operating Temperature Range
Storage Temperature Range
Pin Temperature (Soldering, 10 s)

13.2 V
550 mW
5.0 V
1.0 mA
-20°C to +60°C
-55°C to +125°C
260°C

*plastic
20-60
Q: Q10P*

CONNECTION DIAGRAM 16-PIN DIP (TOP VIEW) PACKAGE OUTLINE 9B

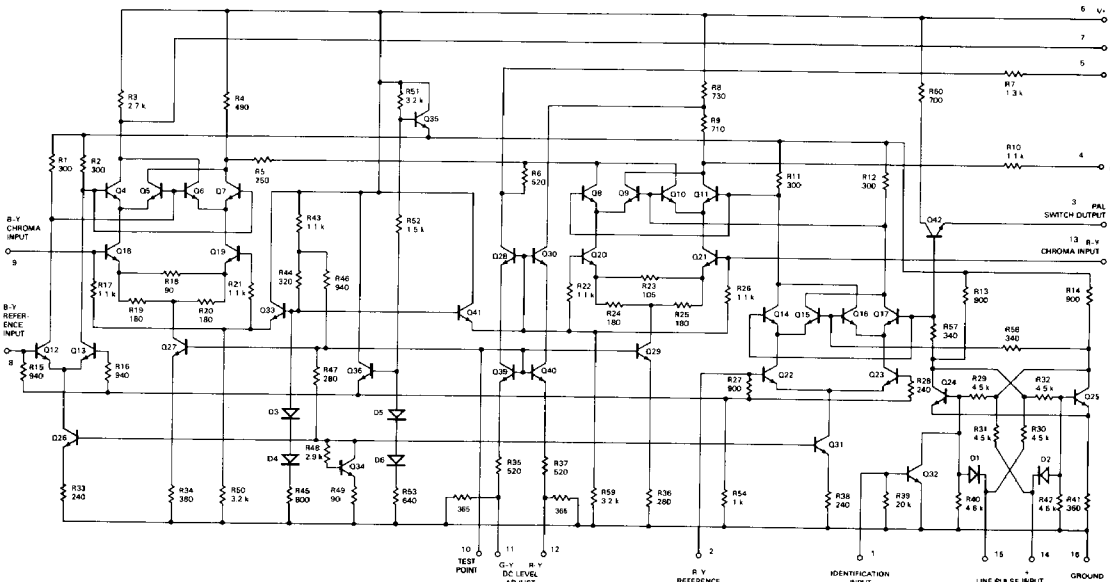


ORDER INFORMATION

TYPE	PART NO.
520	TBA520
(520 Q)	(TBA520 Q)†

†Not recommended for new design.

EQUIVALENT CIRCUIT



*Planar is a patented Fairchild process.

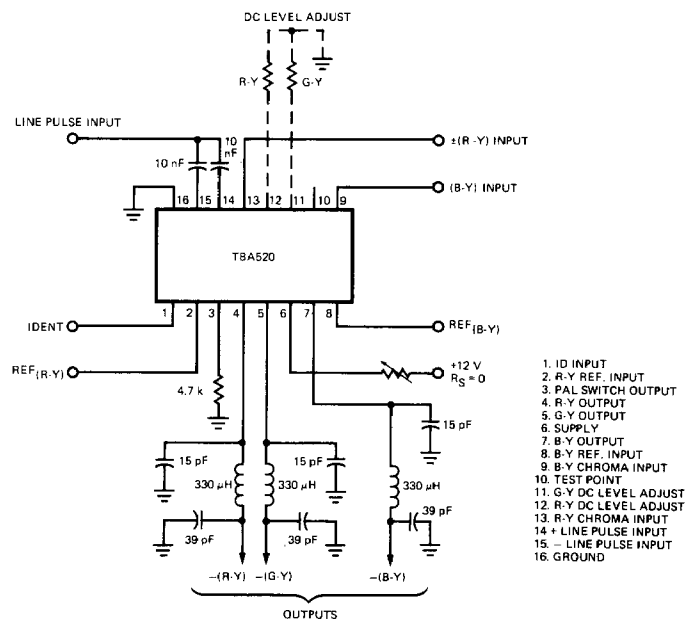
ELECTRICAL CHARACTERISTICS: $T_A = 25^\circ\text{C}$, $V_+ = 12\text{V}$, See Test Circuit, unless otherwise specified.

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current (I_g)			32		mA
Color Difference Gain					
R-Y Channel	$V_g = V_{13} = 50\text{ mV}_{\text{pk-pk}}$, $f = 4.4\text{ MHz}$		7.0		V/V
B-Y Channel			12.5		V/V
G-Y Channel			(Note 1)		
Maximum Color Difference Output Voltage (Notes 2,3)					
R-Y Output (V_4 pk-pk)	(Notes 2,3)		3.2		$V_{\text{pk-pk}}$
B-Y Output (V_7 pk-pk)			4.0		$V_{\text{pk-pk}}$
G-Y Output (V_5 pk-pk)			1.8		$V_{\text{pk-pk}}$
Color Difference dc Output Voltage					
R-Y Output (V_4)			7.9		V
B-Y Output (V_7)			7.9		V
G-Y Output (V_5)			7.9		V
Input Resistance of Chroma Inputs (R9, R13)	$V_g = V_{13} = 20\text{ mV}_{\text{rms}}$ (Sinusoidal)	800			Ω
Input Capacitance of Chroma Inputs (C9, C13)	$f = 4.4\text{ MHz}$			10	pF
Output Resistance at Color Difference Terminals (R4, R5, R7)			2.7		$k\Omega$
Input Resistance of Reference Inputs (R2, R8)			1.0		$k\Omega$
Peak-to-Peak PAL Switch Output Voltage (V_3 pk-pk)	(Note 4)		2.5		$V_{\text{pk-pk}}$
Activation Threshold Voltage (V_1)	Identification Circuit is Active	0.75			V
Activation Threshold Current (I_1)	Identification Circuit is Active	80			μA
Deactivation Threshold Voltage (V_1)	Identification Circuit is Inactive			0.4	V

NOTES:

- G-Y output is typically equal to -0.51 (R-Y) -0.19 (B-Y).
- Gain is equal to 0.7 of small signal gain.
- Reference input ($V_{2\text{pk-pk}}$ and $V_{8\text{pk-pk}}$) range is 0.5 V to 2.0 V.
- $f_{\text{out}} = 0.5 \times$ line pulse frequency; $V_{14} = V_{15} = -3.0\text{ V}$ to -4.5 V (peak).

TEST CIRCUIT



APPLICATION INFORMATION

The function is quoted against the corresponding pin numbers.

1. Identification bias

The input current required to stop the flip-flop, "Ident on": $I_{on} \geq 80 \mu A$. For "Ident off": $V_{off} = -5.0$ to $+0.4$ V.

2. R-Y subcarrier reference input

An 1.0 V peak-to-peak signal is required via a dc blocking capacitor. Under no circumstances should this signal be less than 0.5 V peak-to-peak. The input resistance at this pin is typically 1 k Ω .

3. PAL square wave output The amplitude is 2.5 V peak-to-peak from an emitter follower.

4. R-Y signal output (G-Y at pin 5 and B-Y at pin 7)

No external dc load needed except that direct connection must be made via the low pass filter to the R G B matrix of the TBA530.

The signals produced are in the following ratios:

$$V_{B-Y} = 1.3 V_{R-Y}$$

$$(a) V_{G-Y} = 0.76 V_{R-Y}$$

$$(b) V_{G-Y} = 0.26 V_{R-Y}$$

Condition (a) refers to (B-Y) + (R-Y) addition in the G-Y matrix. Condition (b) refers to the phase reversed (R-Y) input signal where (G-Y) is obtained by subtraction.

The dc levels should each be adjusted, starting with the (B-Y) to $+7.5$ V at nominal supply voltage.

The maximum peak-to-peak voltages for the condition $m \geq 0.7$ (m = ratio of minimum to maximum differential gains) are:

$$V_{R-Y}(pk-pk) = 3.2 \text{ V}$$

$$V_{G-Y}(pk-pk) = 1.8 \text{ V}$$

$$V_{B-Y}(pk-pk) = 4.0 \text{ V}$$

The output impedance for each signal is 2.7 k Ω .

The drifts in dc levels of the color difference output signals for a change in ambient temperature of 40°C (after equilibrium is reached from switch-on) are typically:

$$\text{Absolute shift} \quad -50 \text{ to } +50 \text{ mV}$$

$$V_{R-Y} \text{ relative to } V_{B-Y} \quad -20 \text{ to } +20 \text{ mV}$$

$$V_{G-Y} \text{ relative to } V_{B-Y} \quad -20 \text{ to } +20 \text{ mV}$$

$$V_{R-Y} \text{ relative to } V_{G-Y} \quad -20 \text{ to } +20 \text{ mV}$$

The changes in dc level with supply voltage are approximately linear and track together.

The -3.0 dB bandwidth of the color difference signals is 1.5 MHz.

5. G-Y signal output (see pin 4)

6. Positive supply

Also dc level setting for B-Y output (pin 7). The maximum allowable voltage on this pin is 13.2 V. The minimum supply voltage to insure setting the B-Y output dc level correctly ($+7.5$ V) is 11.6 V (in such case R_S would be set to zero).

7. B-Y signal output (see pin 4)

8. B-Y subcarrier reference input The requirements here are identical with those for pin 2.

9. Chrominance B-Y input signal

An input signal up to 360 mV peak-to-peak (color bars) is advisable. For driving the TBA530 an input signal of 160 mV is required.

10. Internally connected No external connection should be made.

11. DC level setting for G-Y output signal (circuit diagram on page 2).

12. DC level setting for R-Y output (see circuit diagram on page 2).

13. Chrominance R-Y input signal

An input signal up to 500 mV peak-to-peak (color bars) is advisable. The input impedance is the same as for pin 9.

14. Line pulse input (flip-flop synchronizing)

A 4.0 V peak negative going line flyback pulse should be applied via separate 10 nF capacitors to pins 14 and 15. Pulse amplitude to lie between 3.0 V and 4.5 V peak-to-peak.

15. Line pulse input (see pin 14).

16. Ground.

BLOCK DIAGRAM

