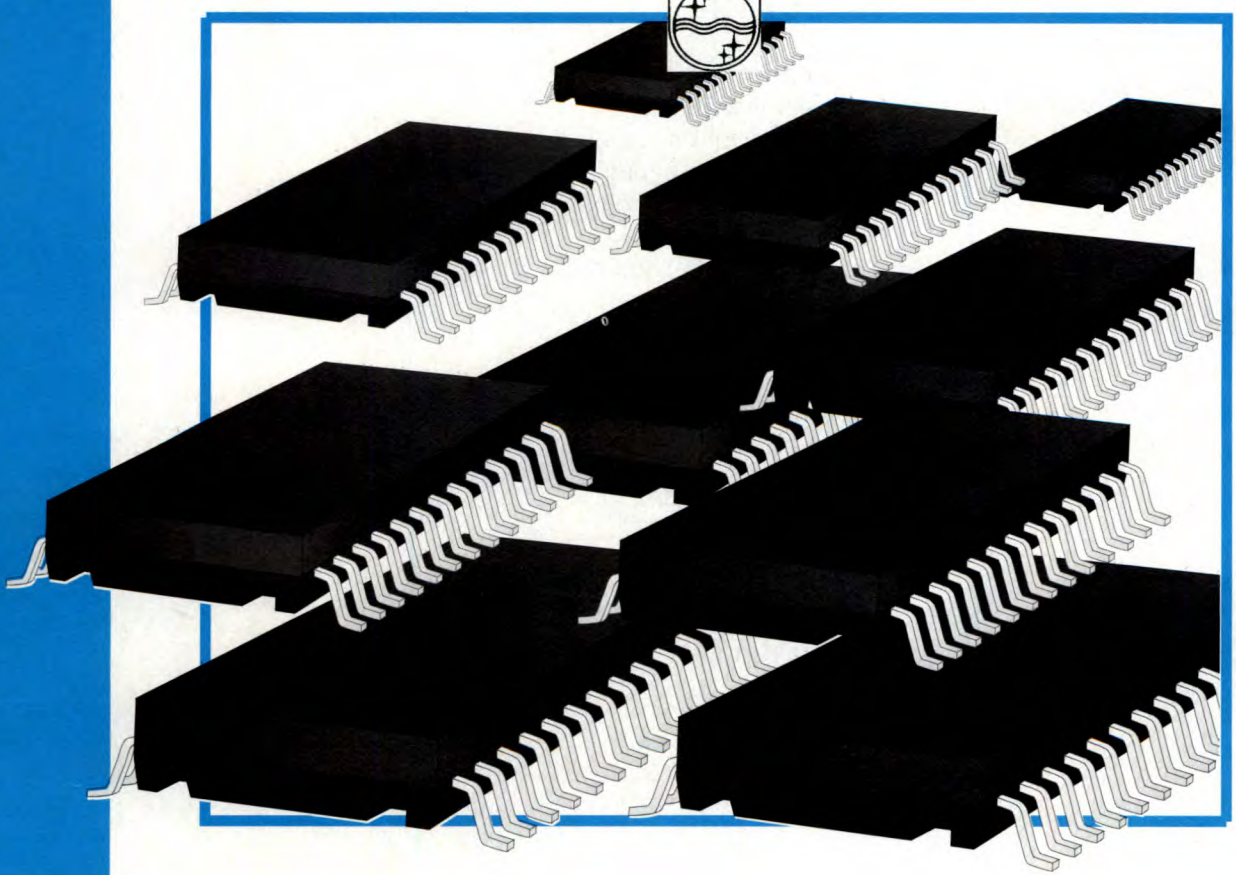
I DATA SHEET DI FARE ELETTRONICA

• LINEARI E TELECOMUNICAZIONI •
• RADIO E SISTEMI AUDIO •
• VIDEO E SISTEMI VIDEO • TTL •

IN COLLABORAZIONE CON PHILIPS



74F166

NE/SE5539

NE/SE5539
AMPLIFICATORE OPERAZIONALE PER ALTE FREQUENZE

DESCRIZIONE

L'NE/SE5539 è un amplificatore operazionale monolitico che, grazie ad un'ampia larghezza di banda e ad un elevato slew rate, si presta molto bene ad essere impiegato in applicazioni di amplificatori video, RF, ed in quelli con un alto slew rate.
Gli ingressi configurati in emitter follower, assicurano una alta impedenza differenziale. Una appropriata compensazione esterna permette la progettazione di una vasta gamma di circuiti ad anello chiuso, sia invertenti che non invertenti, per soddisfare qualsiasi tipo di richiesta.

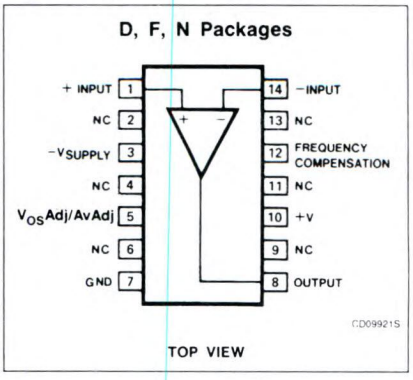
CARATTERISTICHE

- Larghezza di banda
  - guadagno unitario 350 MHz
  - piena potenza 48 MHz
  - GBW 1.2 GHz a 17 dB;
- Slew rate: 600/Vμs;
- A_{VOL}: tipico 52 dB ;
- Low noise tipico - 4 nV/√Hz;
- Dispone del processo MIL-STD.

APPLICAZIONI

- datacomm ad alta velocità;
- monitor video e TV;
- comunicazioni via satellite;
- processo delle immagini;
- strumentazione RF e oscillatori;
- registrazioni magnetiche;
- comunicazioni militari.

PIN CONFIGURATION



ORDERING INFORMATION

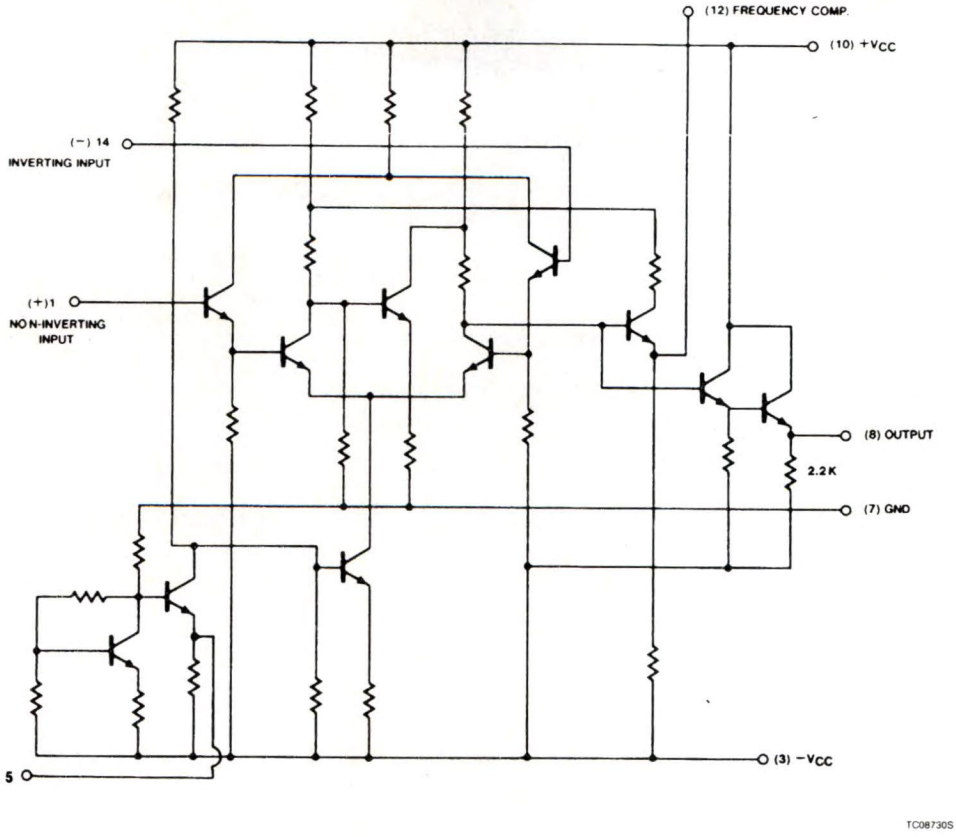
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP	0 to +70°C	NE5539N
14-Pin Plastic SO	0 to +70°C	NE5539D
14-Pin Cerdip	0 to +70°C	NE5539F
14-Pin Plastic DIP	−55°C to +125°C	SE5539N
14-Pin Cerdip	−55°C to +125°C	SE5539F

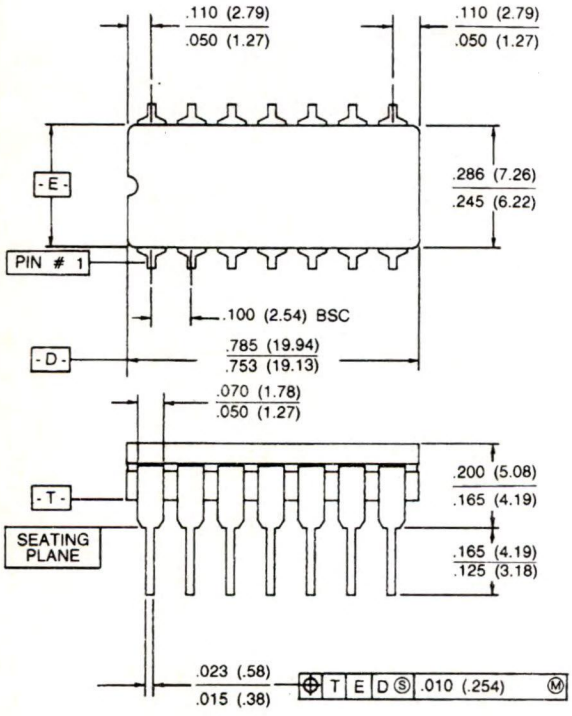
ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	±12	V
P_{DMAX}	Maximum power dissipation, T_A = 25°C (still-air)[2]		
	F package	1.17	W
	N package	1.45	W
	D package	0.99	W
T_{STG}	Storage temperature range	−65 to +150	°C
T_J	Max junction temperature	150	°C
T_A	Operating temperature range		
	NE	0 to 70	°C
	SE	−55 to +125	°C
T_{SOLD}	Lead temperature (10sec max)	300	°C

NOTES:
1. Differential input voltage should not exceed 0.25V to prevent excessive input bias current and common-mode voltage 2.5V. These voltage limits may be exceeded if current is limited to less than 10mA.
2. Derate above 25°C, at the following rates:
   F package at 9.3 mW/°C
   N package at 11.6 mW/°C
   D package at 7.9 mW/°C

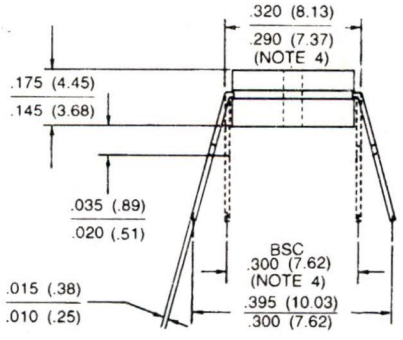
EQUIVALENT CIRCUIT





NOTES:

1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M – 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #14 when viewed from the top.



853-0581 81594

PO00440S

DC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 8V$, $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS		SE5539			NE5539			UNIT
				Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage	$V_O = 0V$, $R_S = 100\Omega$	Over temp		2	5				mV
			$T_A = 25°C$		2	3		2.5	5	
	$\Delta V_{OS}/\Delta T$				5			5		$\mu V/°C$
I_{OS}	Input offset current		Over temp		0.1	3				μA
			$T_A = 25°C$		0.1	1			2	
	$\Delta I_{OS}/\Delta T$				0.5			0.5		nA/°C
I_B	Input bias current		Over temp		6	25				μA
			$T_A = 25°C$		5	13		5	20	
	$\Delta I_B/\Delta T$				10			10		nA/°C
CMRR	Common-mode rejection ratio	F = 1kHz, $R_S = 100\Omega$, $V_{CM} \pm 1.7V$		70	80		70	80		dB
			Over temp	70	80					dB
R_{IN}	Input impedance				100			100		kΩ
R_{OUT}	Output impedance				10			10		Ω

DC ELECTRICAL CHARACTERISTICS (Continued) $V_{CC} = \pm 8V$, $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS			SE5539			NE5539			UNIT
					Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output voltage swing	$R_L = 150\Omega$ to GND and 470Ω to $-V_{CC}$		+Swing				+2.3	+2.7		V
				−Swing				−1.7	−2.2		
V_{OUT}	Output voltage swing	$R_L = 2k\Omega$ to GND	Over temp	+Swing	+2.3	+3.0					V
				−Swing	−1.5	−2.1					
			$T_A = 25°C$	+Swing	+2.5	+3.1					V
				−Swing	−2.0	−2.7					
$I_{CC}+$	Positive supply current	$V_O = 0$, $R_1 = \infty$		Over temp		14	18				mA
				$T_A = 25°C$		14	17		14	18	
$I_{CC}-$	Negative supply current	$V_O = 0$, $R_1 = \infty$		Over temp		11	15				mA
				$T_A = 25°C$		11	14		11	15	
PSRR	Power supply rejection ratio	$\Delta V_{CC} = \pm 1V$		Over temp		300	1000				$\mu V/V$
				$T_A = 25°C$					200	1000	
A_{VOL}	Large signal voltage gain	$V_O = +2.3V, -1.7V$ $R_L = 150\Omega$ to GND, 470Ω to $-V_{CC}$						47	52	57	dB
A_{VOL}	Large signal voltage gain	$V_O = +2.3V, -1.7V$ $R_L = 2\Omega$ to GND									dB
				$T_A = 25°C$				47	52	57	
A_{VOL}	Large signal voltage gain	$V_O = +2.5V, -2.0V$ $R_L = 2k\Omega$ to GND		Over temp	46		60				dB
				$T_A = 25°C$	48	53	58				

DC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 6V$, $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS			SE5539 Min	SE5539 Typ	SE5539 Max	UNIT
V_{OS}	Input offset voltage			Over temp		2	5	mV
				$T_A = 25°C$		2	3	
I_{OS}	Input offset current			Over temp		0.1	3	μA
				$T_A = 25°C$		0.1	1	
I_B	Input bias current			Over temp		5	20	μA
				$T_A = 25°C$		4	10	
CMRR	Common-mode rejection ratio	$V_{CM} = \pm 1.3V$, $R_S = 100\Omega$			70	85		dB
$I_{CC}+$	Positive supply current			Over temp		11	14	mA
				$T_A = 25°C$		11	13	
$I_{CC}-$	Negative supply current			Over temp		8	11	mA
				$T_A = 25°C$		8	10	
PSRR	Power supply rejection ratio	$\Delta V_{CC} = \pm 1V$		Over temp		300	1000	μV/V
				$T_A = 25°C$				
V_{OUT}	Output voltage swing	$R_L = 150\Omega$ to GND and 390Ω to $-V_{CC}$	Over temp	+Swing	+1.4	+2.0		V
				−Swing	−1.1	−1.7		
			$T_A = 25°C$	+Swing	+1.5	+2.0		
				−Swing	−1.4	−1.8		

AC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 8V$, $R_L = 150\Omega$ to GND & 470Ω to $-V_{CC}$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5539 Min	SE5539 Typ	SE5539 Max	NE5539 Min	NE5539 Typ	NE5539 Max	UNIT
BW	Gain bandwidth product	$A_{CL} = 7$, $V_0 = 0.1\ V_{P-P}$		1200			1200		MHz
	Small-signal bandwidth	$A_{CL} = 2$, $R_L = 150\Omega$[1]		110			110		MHz
t_S	Settling time	$A_{CL} = 2$, $R_L = 150\Omega$[1]		15			15		ns
SR	Slew rate	$A_{CL} = 2$, $R_L = 150\Omega$[1]		600			600		V/μs
t_{PD}	Propagation delay	$A_{CL} = 2$, $R_L = 150\Omega$[1]		7			7		ns
	Full power response	$A_{CL} = 2$, $R_L = 150\Omega$[1]		48			48		MHz
	Full power response	$A_V = 7$, $R_L = 150\Omega$[1]		20			20		MHz
	Input noise voltage	$R_S = 50\Omega$, 1MHz		4			4		$nV/\sqrt{Hz}$
	Input noise current	1MHz		6			6		$pA/\sqrt{Hz}$

NOTE:
1. External compensation.

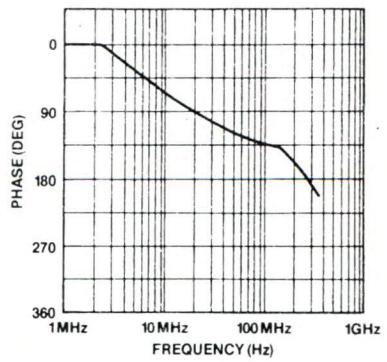
AC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 6V$, $R_L = 150\Omega$ to GND and 390Ω to $-V_{CC}$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5539			UNIT
			Min	Typ	Max	
BW	Gain bandwidth product	$A_{CL} = 7$		700		MHz
	Smali-signal bandwidth	$A_{CL} = 2^1$		120		MHz
t_S	Settling time	$A_{CL} = 2^1$		23		ns
SR	Slew rate	$A_{CL} = 2^1$		330		V/μs
t_{PD}	Propagation delay	$A_{CL} = 2^1$		4.5		ns
	Full power response	$A_{CL} = 2^1$		20		MHz

NOTE:
1. External compensation.

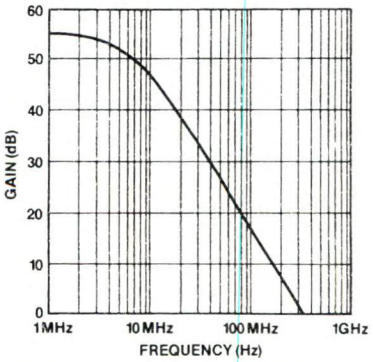
TYPICAL PERFORMANCE CURVES

NE5539 Open-Loop Phase



OP20520S

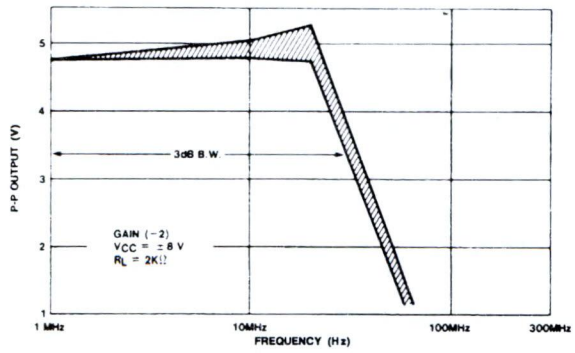
NE5539 Open-Loop Gain



OP20530S

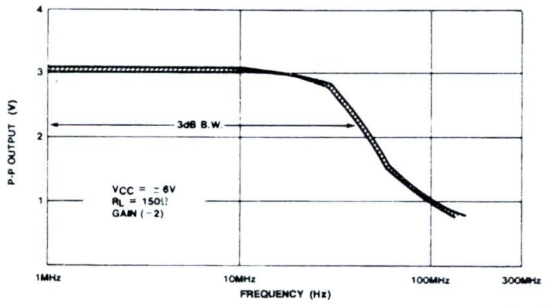
TYPICAL PERFORMANCE CURVES (Continued)

Power Bandwidth (SE)



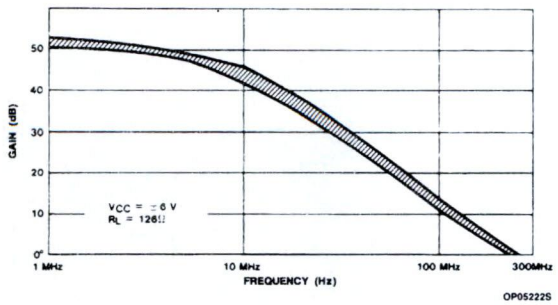
OP05202S

Power Bandwidth (NE)



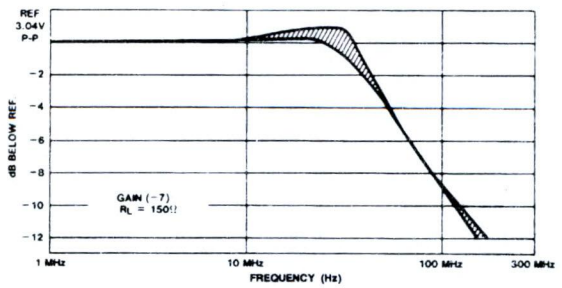
OP05212S

SE5539 Open-Loop Gain vs Frequency



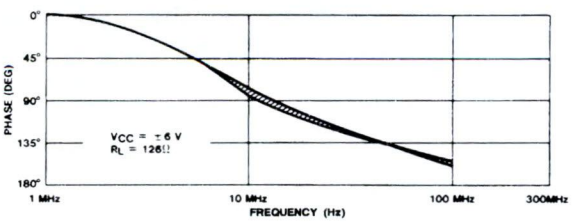
OP05222S

Power Bandwidth

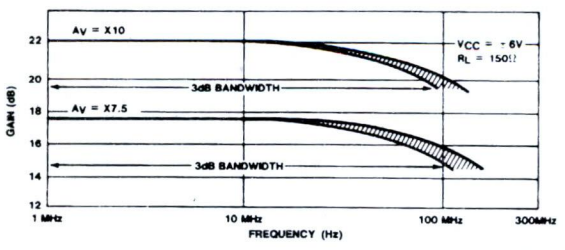


OP05231S

SE5539 Open-Loop Phase vs Frequency



Gain Bandwidth Product vs Frequency



OP05251S

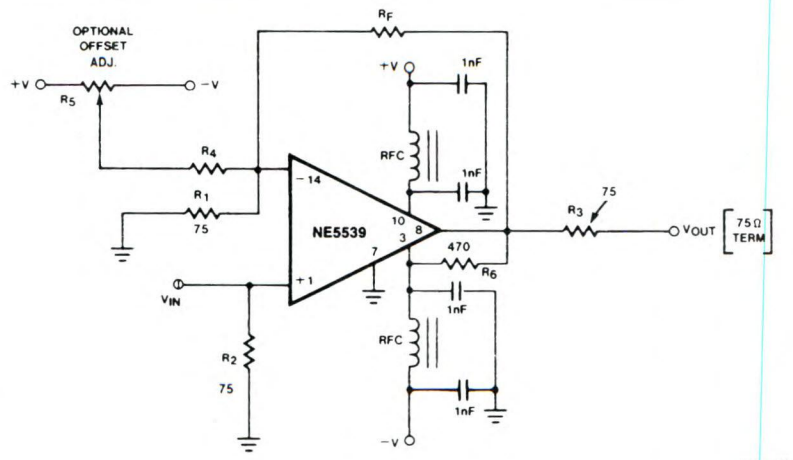
NOTE

Indicates typical distribution $-55°C \leq T_A \leq 125°C$

OP05241S

CONSIDERAZIONI SUL LAYOUT DEL CIRCUITO

Come si può facilmente immaginare, lavorando a frequenze molto alte con un amplificatore a larga banda, sorgono problemi di instabilità e il progetto del circuito è molto critico. Il breadbording non è assolutamente da scartare. Un circuito stampato a doppia faccia con fori metallizzati è la soluzione ideale per tutte le applicazioni. In Figura 1 viene mostrato un esempio di amplificatore a 28 dB non invertente.

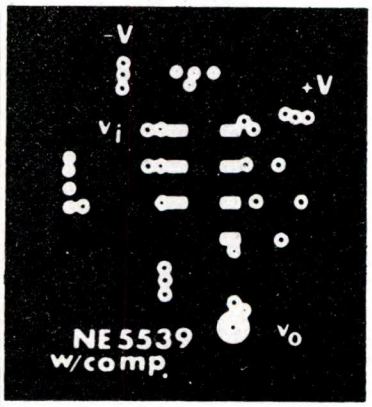


NOTES:
R_1 = 75Ω 5% CARBON
R_2 = 75Ω 5% CARBON
R_3 = 75Ω 5% CARBON
R_4 = 36k 5% CARBON

R_5 = 20k TRIMPOT (CERMET)
R_F = 1.5k (28dB GAIN)
R_6 = 470Ω 5% CARBON

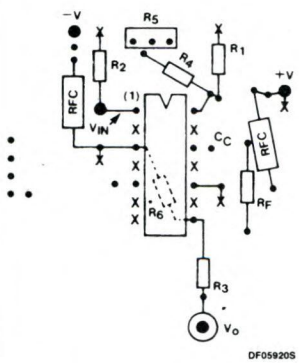
RFC 3T # 26 BUSS WIRE ON FERROXCUBE VK 200 09/3B CORE
BYPASS CAPACITORS
1nF CERAMIC
(MEPCO OR EQUIV.)

Top Plane Copper[1] (Component Side)



DF05910S

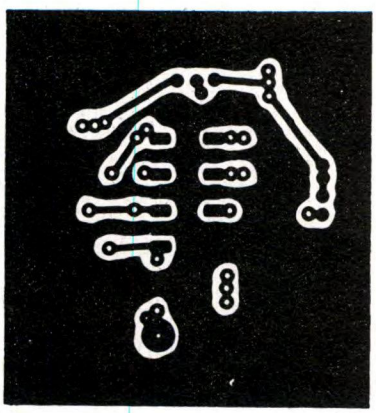
Component Side (Component Layout)



DF05920S

NOTES:
(X) indicates ground connection to top plane.
*R_6 is on bottom side.

Bottom Plane Copper[1]



DF05930S

NOTE:
1. Bond edges of top and bottom ground plane copper.

Figura 1. Layout di un amplificatore non invertente a 28 dB.

NE5539 COME AMPLI VIDEO A COLORI

L'amplificatore operazionale a larga banda NE5539 può essere facilmente adattato per essere utilizzato come amplificatore video a colori. Un esempio tipico di circuito applicativo viene mostrato in **Figura 2** assieme all'immagine dei vector-scope[1] che mostra il guadagno differenziale dell'amplificatore e le fasi di risposta ad un segnale a scalino modulato in cinque passi (**Figure 3, 4 e 5**). Come si può vedere, il guadagno varia di meno del 0,5% dal basso all'alto della scala. La massima fase differenziale, mostrata in figura 5, è approssimativamente +0,1°C.
Il circuito dell'amplificatore è stato ottimizzato per operare con un'impedenza terminale di 75Ω in ingresso e in uscita con un guadagno che si aggira attorno a 10 (20 dB).

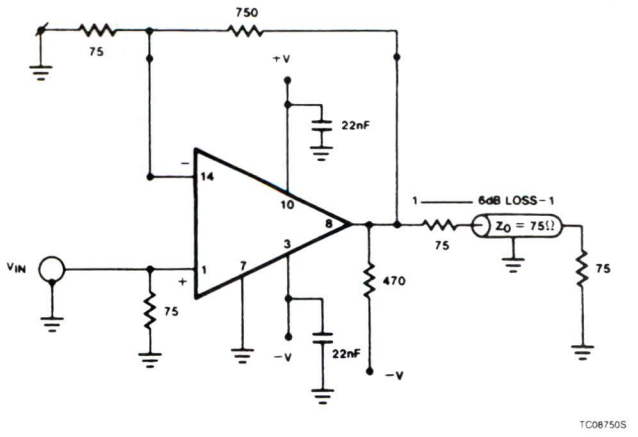


Figura 2. Amplificatore video con NE5539.

NOTA:
1. Con segnale d'ingresso di 200 mV e segnale d'uscita di 2 V. La tensione di alimentazione è V_{CC} = ±8V.

NOTA: queste misure sono state realizzate con un generatore di segnali Tektronix 146 NTSC,un vectorscope 520A NTSC e il monitor waveform 1480.

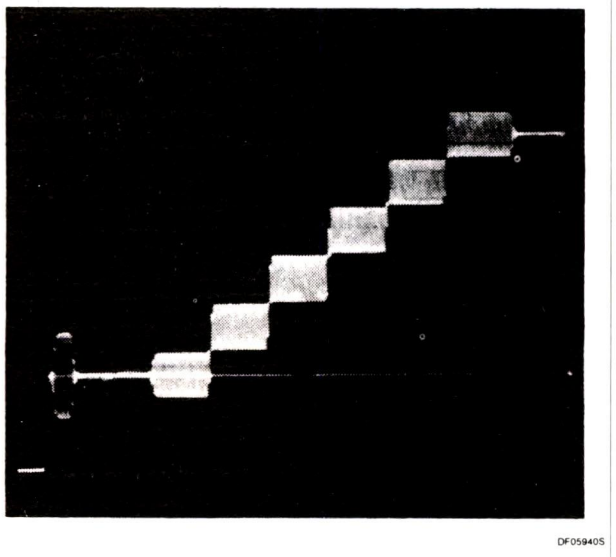


Figura 3. Segnale d'ingresso.

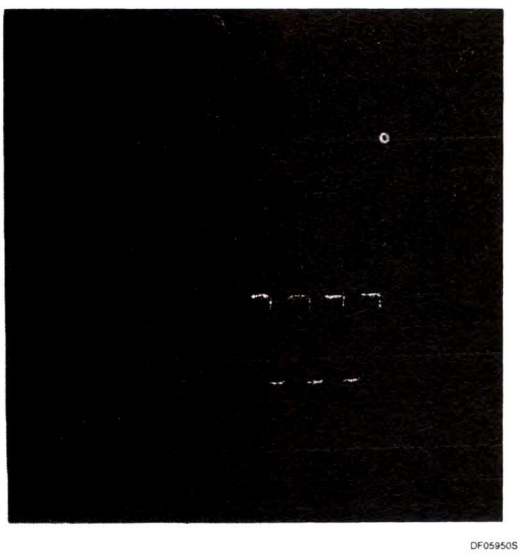


Figura 4. Guadagno differenziale <0.5%.

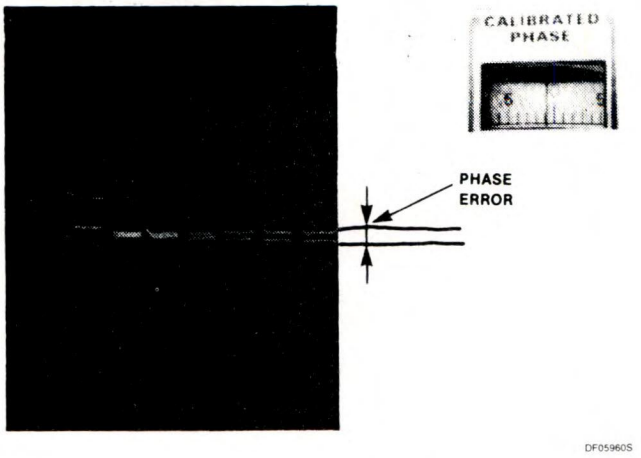


Figura 5. Fase differenziale +0.1°.

APPLICAZIONI

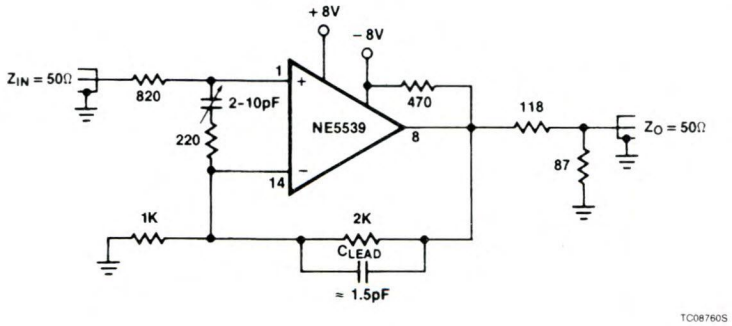


Figura 6. Follower non invertente.

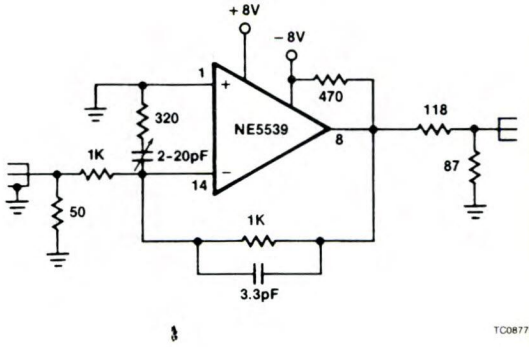


Figura 7. Follower invertente.

74F166: SHIFT REGISTER UNIVERSALE BIDIREZIONALE 8-BIT

CARATTERISTICHE

- Alta impedenza d'ingresso degli stadi NPN per ridurre il carico (20 µA negli stati alto e basso);
- Applicazione da parallelo a seriale sincrono.
- Ingresso dati seriale sincrono per una più facile espansione.
- Abilitazione clock inl modo "do nothing".
- Master reset asincrono.
- Espandibile a 16 bit con passi da 8 bit.
- Gamma di temperature industriali (da -40°C a +85°C).

TYPE	TYPICAL f_{max}	TYPICAL SUPPLY CURRENT(TOTAL)
74F166	175MHz	50mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V ±10%, T_{amb} = –40°C to +85°C
16–pin plastic DIP	N74F166N	I74F166N
16–pin plastic SO	N74F166D	I74F166D

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

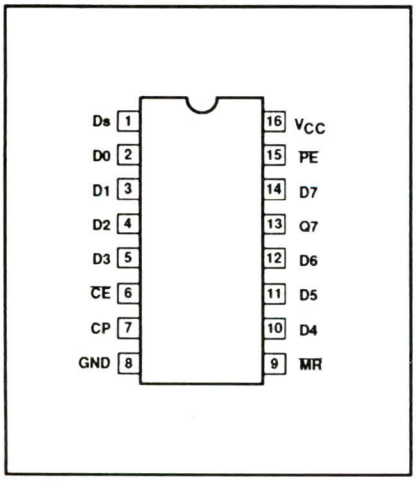
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 – D7	Parallel data inputs	1.0/0.033	20µA/20µA
Ds	Serial data input (shift right)	2.0/0.066	40µA/40µA
CP	Clock input (active rising edge)	1.0/0.033	20µA/20µA
$\overline{CE}$	Clock enable input (active low)	1.0/0.033	20µA/20µA
$\overline{PE}$	Parallel enable input (active low)	1.0/0.033	20µA/20µA
$\overline{MR}$	Master reset input (active low)	2.0/0.066	40µA/40µA
Q7	Data output	50/33	1.0mA/20mA

Note to input and output loading and fan out table
1. One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

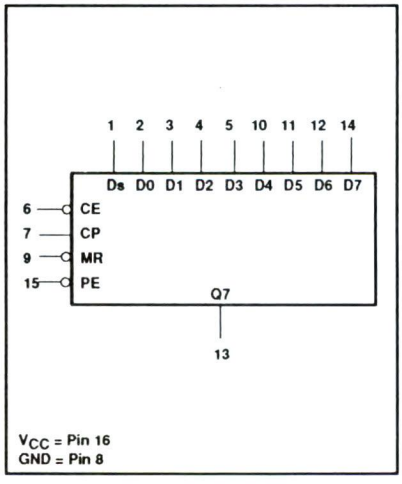
DESCRIZIONE

Il 74F166 è uno shift register a 8 bit veloce in grado di gestire dati seriali e paralleli in modo sincrono per mezzo di un ingresso parallelo attivo basso ($\overline{PE}$). Per tutto il tempo in cui $\overline{PE}$ si trova a livello logico basso prima della transizione low-to-high del segnale di clock, i dati paralleli vengono inseriti nel registro. Quando PE si trova allo stato logico alto, i dati vengono trasferiti nella locazione interna Q0, dall'ingresso dati seriale (Ds), e i bit rimanenti vengono fatti slittare di una posizione verso destra (Q0 --> Q1 --> Q2, ecc.) ad ogni fronte di salita del segnale. Per i l'espansione dei registri nei convertitori parallelo-seriale, l'uscita Q7 è collegata all'ingresso Ds dello stadio successivo. L'ingresso del clock viene combinato per mezzo di una porta OR in modo da mettere a disposizione l'ingresso active-low di abilitazione $\overline{CE}$. L'assegnazione dei terminali degli ingressi CP e $\overline{CE}$ è arbitraria e può essere invertita a seconda di come viene realizzato il layout del circuito. La transizione low-to-high dell'ingresso $\overline{CE}$ avviene solo se CP va altoi. Un livello basso all'ingresso master reset ($\overline{MR}$) azzeragli ingressi e cancella il registro asincrono, forzando tutte le locazioni in low state.

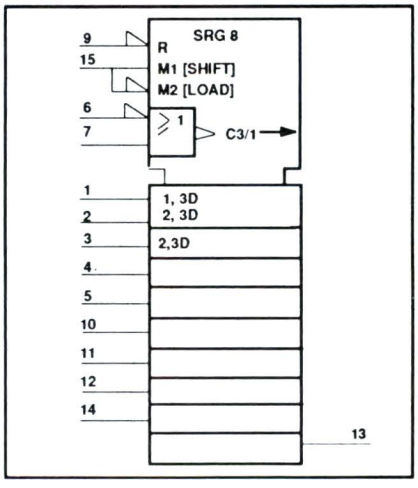
PIN CONFIGURATION



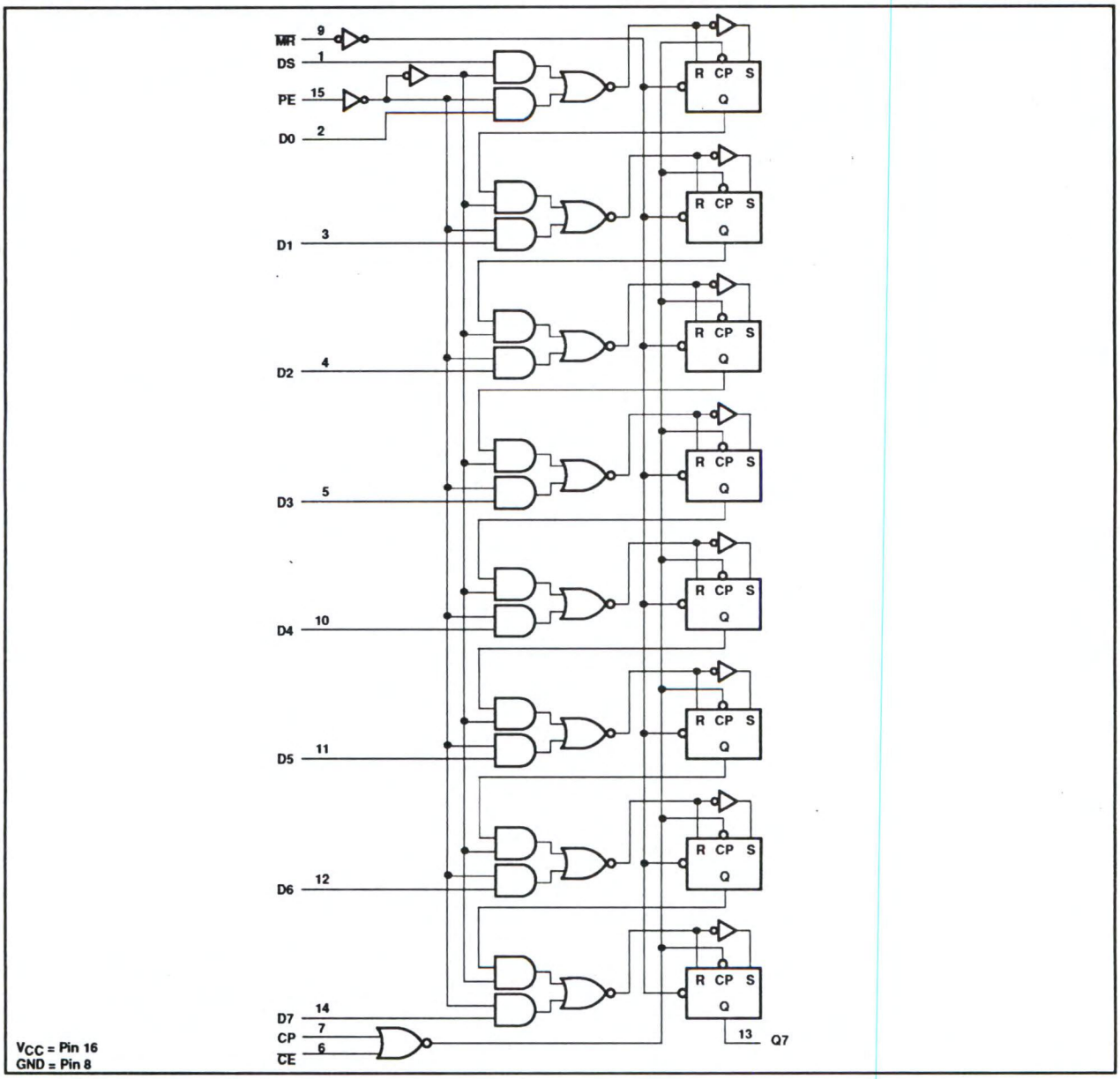
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS					Qn REGISTER		OUTPUT	OPERATING MODE
PE	$\overline{CE}$	CP	DS	D0 –D7	Q0	Q1 – Q6	Q7	
l	l	↑	X	l – l	L	L – L	L	Parallel load
l	l	↑	X	h – h	H	H – H	H	
h	l	↑	l	X – X	L	q0 – q5	q6	Serial shift
h	l	↑	h	X – X	H	q0 – q5	q6	
X	h	X	X	X – X	qn	q1 – q6	q7	Hold (do nothing)

Notes to function table

1. H = High–voltage level

2. h = High voltage level one setup time before the low–to–high clock transition
3. L = Low–voltage level
4. l = Low voltage level one setup time before the low–to–high clock transition
5. qn = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the low–to–high clock transition
6. X = Don't care
7. ↑ = Low–to–high clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state		40	mA
T_{amb}	Operating free air temperature range	Commercial range	0 to +70	°C
		Industrial range	–40 to +85	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IN}	High–level input voltage		2.0			V
V_{IL}	Low–level input voltage				0.8	V
I_{Ik}	Input clamp current				–18	mA
I_{OH}	High–level output current				–1	mA
I_{OL}	Low–level output current				20	mA
T_{amb}	Operating free air temperature range	Commercial range	0		+70	°C
		Industrial range	–40		+85	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS MIN	LIMITS TYP[2]	LIMITS MAX	UNIT
V_{OH}	High–level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = MAX	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
V_{OL}	Low–level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = MAX	±10%V_{CC}		0.30	0.50	V
					±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	others	V_{CC} = 0.0V, V_I = 7.0V					100	µA
		$\overline{CE}$, CP[3]							
I_{IH}	High–level input current	others	V_{CC} = MAX, V_I = 2.7V					20	µA
		$\overline{MR}$, Ds						40	µA
		Industrial only: others						40	µA
		Industrial only: $\overline{MR}$, Ds						80	µA
I_{IL}	Low–level input current	others	V_{CC} = MAX, V_I = 0.5V					-20	µA
		$\overline{MR}$, Ds						-40	µA
I_{OS}	Short–circuit output current[4]		V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX, $\overline{PE}$ = $\overline{CE}$ = Dn = GND, $\overline{MR}$ = Ds = 4.5V, CP = ↑				50	70	mA

Notes to DC electrical characteristics

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. When testing CP, $\overline{CE}$ must remain in high state, whereas CP must remain in high state when testing $\overline{CE}$.
4. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

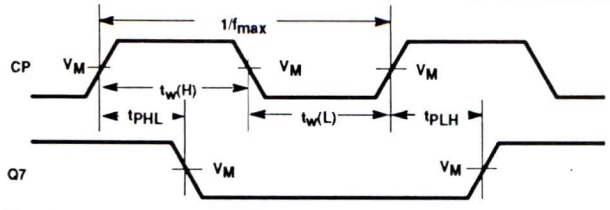
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS: T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			LIMITS: T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		LIMITS: T_{amb} = –40°C to +85°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	Waveform 1	135	175		110		100		ns
t_{PLH} t_{PHL}	Propagation delay CP to Q7	Waveform 1	5.0 4.0	7.5 6.0	10.0 8.0	5.0 3.5	12.0 9.0	5.0 3.5	13.0 9.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q7	Waveform 2	4.0	6.5	8.5	4.0	9.5	4.0	9.5	ns

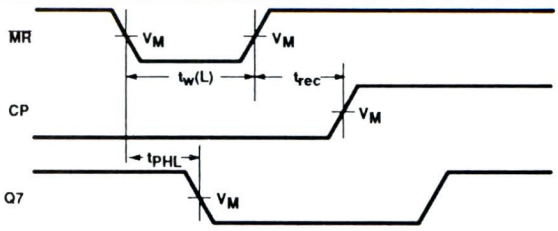
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		T_{amb} = –40°C to +85°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{su} (H) t_{su}(L)	Setup time, high or low Dn, Ds to CP, $\overline{CE}$	Waveform 3	3.0 2.5			4.0 3.0		4.0 3.0		ns
t_h (H) t_h (L)	Hold time, high or low Dn, Ds to CP	Waveform 3	0.0 0.0			1.0 0.0		1.0 0.0		ns
t_h (H) t_h (L)	Hold time, high or low Dn, Ds to $\overline{CE}$	Waveform 3	1.5 0.0			2.0 0.0		2.0 0.0		ns
t_{su}(L)	Setup time, low $\overline{CE}$ to CP	Waveform 3	5.0			6.0		6.0		ns
t_h (H)	Hold time, high $\overline{CE}$ to CP	Waveform 3	0.0			0.0		0.0		ns
t_{su} (H) t_{su}(L)	Setup time, high or low $\overline{PE}$ to CP, $\overline{CE}$	Waveform 3	3.0 3.0			4.0 4.0		4.0 6.0		ns
t_h (H) t_h (L)	Hold time, high or low $\overline{PE}$ to CP	Waveform 3	0.0 0.0			0.0 0.0		0.0 0.0		ns
t_w (H) t_w (L)	CP pulse width, high or low	Waveform 1	3.0 4.5			3.5 5.0		3.5 6.0		ns
t_w (L)	$\overline{MR}$ pulse width, low	Waveform 2	4.0			4.0		4.0		ns
t_{rec}	Recovery time $\overline{MR}$ to CP	Waveform 2	4.0			4.5		4.5		ns

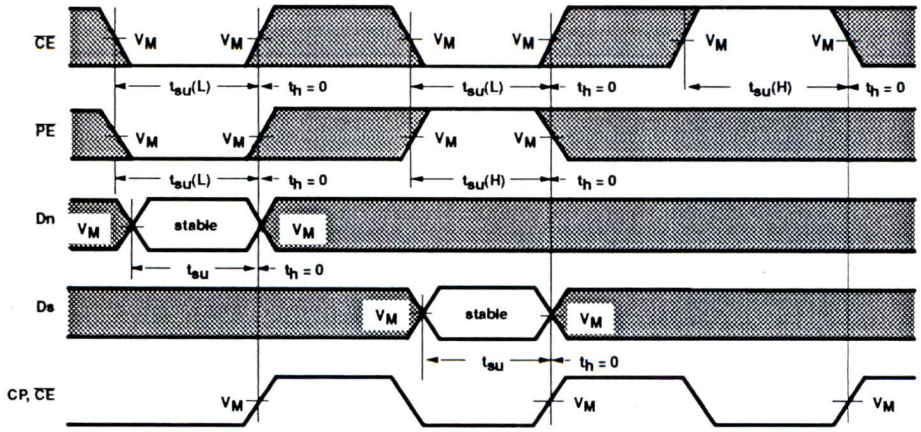
AC WAVEFORMS



Waveform 1. Propagation delay for clock input to output, clock pulse width, and maximum clock frequency



Waveform 2. Master reset pulse width, master reset to output delay and master reset to clock recovery time

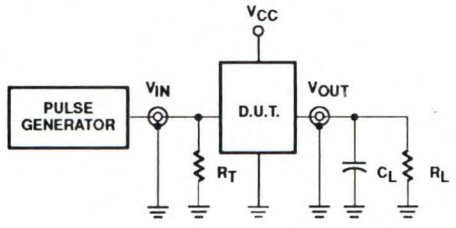


Waveform 3. Setup and hold times

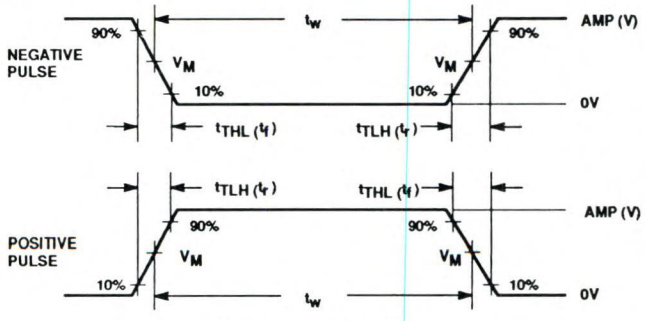
Notes to AC waveforms

1. For all waveforms, V_M = 1.5V.
2. The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test circuit for totem-pole outputs



Input pulse definition

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns